This listing of claims will replace all prior versions and listings of claims in the application:

1-3. (canceled)

4. (currently amended) Apparatus for use in a reduced clock rate finite impulse response filter comprising:

i) Q latch means all coupled to an input data signal having a unit interval rate and each latch means providing a latched output signal in response to a latch control signal;

ii) Q multiplexer/multiplier (mux/mul) means, each mux/mul means providing one output and Q inputs to receive the latched output signal of a respective latch means; ~~and~~

iii) selection means for controlling said mux/mul means operative to produce an output signal selected from one of said Q inputs~~.~~;

iv) means to produce a clock signal; and

v) Q phase delay means coupled to said clock signal providing an output latch control signal to a corresponding latch means;

wherein each phase delay means produces a unique output latch control signal that is phase delayed from the clock signal by a phase delay of N x 360/Q, where unique values of N correspond to each individual phase delay means and range from 0 to Q-1.

5. (original) The apparatus of claim 4 further including:

i) signal conditioning means for each mux/mul means to condition the output signal of the mux/mul means; and

ii) summing means to sum the conditioned signals of all such signal conditioning means.

6. (original) The apparatus of claim 5 wherein said signal conditioning means modifies the gain and the sign of the output signal of the corresponding mux/mul means.

7. (canceled)

8. (canceled)

9. (currently amended) The apparatus of claim ~~7~~ 4, wherein the means to produce a clock signal

operates to produce a clock signal that is a sub-multiple Q of the unit interval rate of said input data signal.

10. (original) The apparatus of claim 4 wherein the selection means operates to select an output signal from one of said Q inputs at a rate corresponding to the unit interval rate of said input data signal.

11. (canceled)

12. (currently amended) A method for providing a feed forward equalizer (FFE) in a transversal finite impulse response (FIR) filter for transmitting data bits that are shifted through delay elements, ~~at a reference clock rate defining a unit interval period and~~ each delay element ~~is~~ being coupled to a corresponding multiplier and all of the multiplied outputs are summed, the method comprising: ~~the steps of:~~

i) supplying the data bits to be processed to Q shift registers operating at a shift rate that is the quotient of the reference clock rate divided by Q; and

ii) multiplexing said Q shift registers to a FIR FFE multiplier summing network for a unit interval period defined by said reference clock rate such that each shift register of said Q shift registers is successively multiplexed to the FIR FFE multiplier summing network in successive unit interval periods.

13. (currently amended) A method for providing a decision feedback equalizer (DFE) in a transversal finite impulse response (FIR) filter for recovering data bits in a received data signal having a data rate defining a unit interval period comprising: ~~the steps of:~~

i) conditioning the received data signal;

ii) supplying the conditioned data signal to Q shift registers of a DFE network, all said shift registers operating at a shift rate that is the quotient of the clock rate of the received data signal divided by Q; and

iii) multiplexing said Q shift registers to a FIR DFE multiplier summing network_for a unit interval period defined by said clock rate of the received data signal such that each shift register of said Q shift registers is successively multiplexed to the FIR DFE multiplier summing network in successive unit interval periods.